ABSTRACT OF THE DISCLOSURE

[0038] An electronic integrated circuit includes a first signal (A1) generated by a first source block (10) and a second signal (B1) generated by a second source block (12). A variable delay circuit (18) detects a delay between said first and second signals in calibration mode and applies the delay to the first signal during normal operation of the circuit. A fixed delay buffer (32) may be used to apply a delay to the second signal to compensate for known delays associated with the variable delay circuit (18).